Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (original): A semiconductor device, comprising:

a P-channel MOS field-effect transistor comprising,

a semiconductor substrate;

a gate dielectric on the substrate; and

a calcium and boron doped polysilicon gate electrode on the gate dielectric.

Claim 2 (original): The semiconductor device of claim 1 wherein the calcium and boron dopants are present in the polysilicon in a ratio of about 1:4 to 1:1.

Claim 3 (original): The semiconductor device of claim 1, wherein the calcium and boron dopants are present in the polysilicon in a ratio of about 1:1.

Claim 4 (original): The semiconductor device of claim 1, wherein the calcium is substantially uniformly distributed throughout the polysilicon gate electrode.

Claim 5 (original): The semiconductor device of claim 1, wherein the calcium is substantially concentrated at or near the polysilicon gate electrode/gate dielectric interface.

Claim 6 (original): The semiconductor device of claim 5, wherein the calcium is at least partially integrated in the polysilicon crystal structure.

Claim 7 (currently amended): The semiconductor device of claim 5, wherein the calcium is [[present in]] **doped into the polysilicon gate electrode such that it forms** a thin atomic layer at the gate electrode/gate dielectric interface.

Claim 8 (original): The semiconductor device of claim 6, wherein the calcium dopant dose is about 0.5e15/cm^2 to 2e15 /cm^2.

Claim 9 (original): The semiconductor device of claim 1, wherein the device is a CMOS device.

Claim 10 (original): The semiconductor device of claim 1, wherein the device is a PMOS device.

Claim 11 (original): A method of making a semiconductor device having a P-channel MOS field-effect transistor, the method comprising:

providing a semiconductor substrate;

forming a gate dielectric layer on the substrate; and

forming a calcium and boron doped polysilicon gate electrode layer on the gate dielectric.

Claim 12 (original): The method of claim 11, further comprising:

patterning and etching the polysilicon and dielectric layers layer to form a gate electrode;

implanting the substrate with dopant to form source and drain regions.

Claim 13 (original): The method of claim 11, wherein the polysilicon gate electrode layer formation comprises:

depositing a layer of boron doped polysilicon on the gate dielectric layer;

implanting the deposited polysilicon with calcium such that the calcium is substantially concentrated at the polysilicon/dielectric interface.

Claim 14 (original): The method of claim 13, wherein the polysilicon layer is deposited to its full thickness prior to calcium implantation.

Claim 15 (original): The method of claim 13, wherein the polysilicon layer is about 1000 to 1500 Å thick.

Claim 16 (original): The method of claim 13, wherein the calcium implantation is conducted at a dose of about 0.5e15/cm^2 to 2e15/cm^2.

Claim 17 (original): The method of claim 13, wherein the polysilicon gate electrode layer formation comprises:

forming a first thin layer of polysilicon on the gate dielectric layer;

implanting the calcium into the first layer of polysilicon; and

forming a second layer of polysilicon over the calcium doped first layer.

Claim 18 (original): The method of claim 17, wherein the first layer of polysilicon is about 100 – 200 Å thick.

Claim 19 (original): The method of claim 18, wherein the second layer of polysilicon is 800 – 1400 Å thick.

Claim 20 (original): The method of claim 18, wherein the calcium implantation is conducted at a dose of about 0.2e15/cm^2 to 1e15/cm^2 and an energy of about 1-5 keV.

Claim 21 (original): The method of claim 11, wherein the polysilicon gate electrode layer formation comprises:

depositing a layer of undoped polysilicon on the gate dielectric layer;

implanting the deposited polysilicon with boron and calcium.

Claim 22 (original): The method of claim 21, wherein boron implantation precedes calcium implantation.

Claim 23 (original): The method of claim 21, wherein calcium implantation precedes boron implantation.

Claim 24 (original): The method of claim 11, wherein the polysilicon gate electrode layer formation comprises:

depositing a layer of calcium doped polysilicon on the gate dielectric layer;

implanting the deposited polysilicon with boron.

Claim 25 (original): The method of claim 11, wherein the polysilicon gate electrode layer formation comprises:

depositing a first thin layer of calcium doped polysilicon on the gate dielectric layer;

depositing a second thicker layer of polysilicon on the first layer;

implanting the deposited polysilicon layers with boron.

Claim 26 (original): The method of claim 11, wherein the polysilicon gate electrode layer formation comprises:

depositing a layer of boron and calcium doped polysilicon on the gate dielectric layer.

Claim 27 (new): A semiconductor device, comprising:

a P-channel MOS field-effect transistor comprising,

a semiconductor substrate;

a gate dielectric on the substrate;

a calcium doped gate electrode on the gate dielectric; and

a thin atomic layer of calcium at an interface between the gate electrode and gate dielectric.